FIG. 3a

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC. NAMELY. HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. ~~MCYO~~ mcyc INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	$\overline{\text{DRAW}}$	INPUT	$\overline{\text{DRAW}}$ SIGNAL FROM ACRTC IS INPUTTED. $\overline{\text{DRAW}}$ INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. $\overline{\text{DRAW}}$ IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	$\overline{\text{AS}}$	INPUT	$\overline{\text{AS}}$ SIGNAL IS INPUTTED FROM ACRTC $\overline{\text{AS}}$ INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	$\overline{\text{HSYNC}}$	INPUT	$\overline{\text{HSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF $\overline{\text{HSYNC}}$ = "LOW" AND $\overline{\text{DRAW}}$ = "HIGH", IF AS PULSE IS RECEIVED, $\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH OPERATION IS CARRIED OUT.
	67	$\overline{\text{VSYNC}}$	INPUT	$\overline{\text{VSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. RECEIVED $\overline{\text{VSYNC}}$ IS DIVIDED BY TWO SO AS TO OUTPUTTED AS VSYNC/2 SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	$\overline{\text{DISP 1}}$	INPUT	$\overline{\text{DISP 1}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{DISP 1}}$ INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	$\overline{\text{CUD1}}$	INPUT	$\overline{\text{CUD 1}}$ SIGNAL IS INPUTTED FROM ACRTIC. $\overline{\text{CUD 1}}$ IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6–10 16 19–28	MAD0 –MAD15	INPUT/OUTPUT	MOD0–MAD15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC = "LOW", AS DATA INPUT/OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC = "HIGH".
	29-32	MA16– MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16 – MA19 IS INPUTTED FROM ACRTC.

FIG. 3b

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	$\overline{RAS}$	OUTPUT	$\overline{RAS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	$\overline{CS}$	OUTPUT	$\overline{CS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	$\overline{WE}$	OUTPUT	$\overline{WE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	$\overline{OE}$	OUTPUT	$\overline{OE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0-FA9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF0-VCF3 AND VMD0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FD0-FD7	INPUT/OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD0-FD3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD0-FD7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 ~~AND~~ 4. DIVISION RATIO IS SET DEPENDING ON VCF0-VCF3 OF ATTRIBUTE CODE. — OR
	33,34 36,37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-DSIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY ~~SHIFTEN~~ OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF0-VCF3. — SHFTEN
	5	SHFTEN ~~SHIFTEN~~	SHFTEN OUTPUT	~~SHIFEN~~ INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, $\overline{DISP1}$ FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, $\overline{DISP1}$ IS ELONGATED BACKWARD BY TWO CYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC/2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. $\overline{VSYNC}$ IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	$\overline{BL2IRQ}$	OUTPUT	$\overline{BL2IRQ}$ IS SET BY BLINK2(MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK2 IS AT "HIGH" LEVEL, ~~BLINK2~~ IS SET TO "LOW" LEVEL. — $\overline{BL2IRQ}$
	39	$\overline{IRQCLR}$	INPUT	$\overline{IRQCLR}$ SIGNAL IS USED TO CLEAR $\overline{BL2IRQ}$ SIGNAL. WHEN "LOW" IS INPUTTED TO $\overline{IRQCLR}$, $\overline{BL2IRQ}$ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

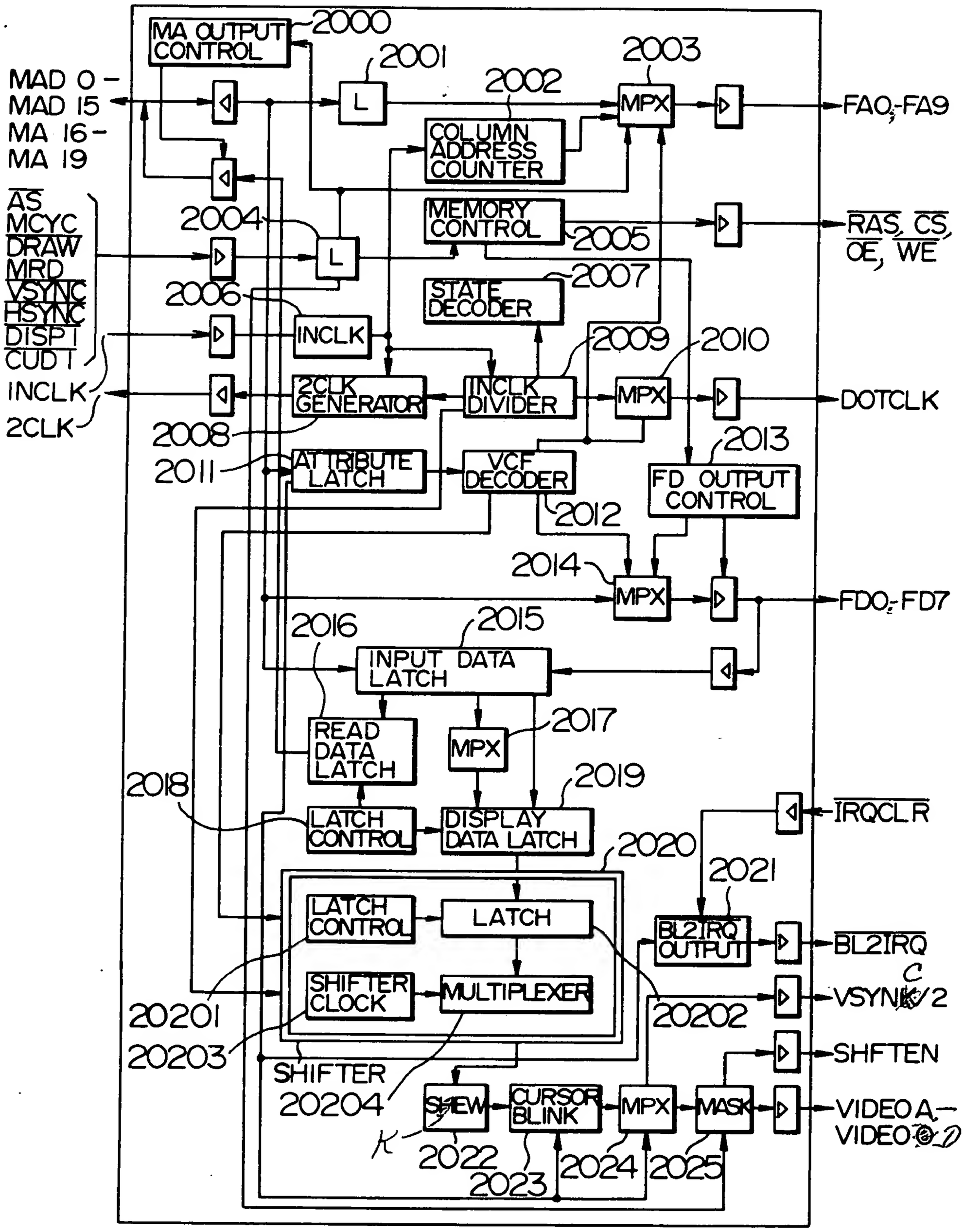
MA OUTPUT CONTROL
2000
2001
2002
2003
MAD 0 - MAD 15
MA 16 - MA 19
L
MPX
FA0 - FA9
COLUMN ADDRESS COUNTER
MEMORY CONTROL
2005
RAS, CS, OE, WE
AS
MCYC
DRAW
MRD
VSYNC
HSYNC
DISPT
CUDT
INCLK
2CLK
2004
2006
2007
STATE DECODER
INCLK
2CLK GENERATOR
INCLK DIVIDER
2009
2010
DOTCLK
2008
2011
ATTRIBUTE LATCH
VCF DECODER
2012
2013
FD OUTPUT CONTROL
2014
FD0 - FD7
2016
2015
INPUT DATA LATCH
READ DATA LATCH
2017
2018
2019
LATCH CONTROL
DISPLAY DATA LATCH
IRQCLR
2020
2021
BL2IRQ OUTPUT
BL2IRQ
20201
20202
20203
SHIFTER CLOCK
MULTIPLEXER
VSYNC2
SHFTEN
SHIFTER
20204
SKEW
CURSOR BLINK
MASK
VIDEO A - VIDEO D
2022
2023
2024
2025

FIG. 7

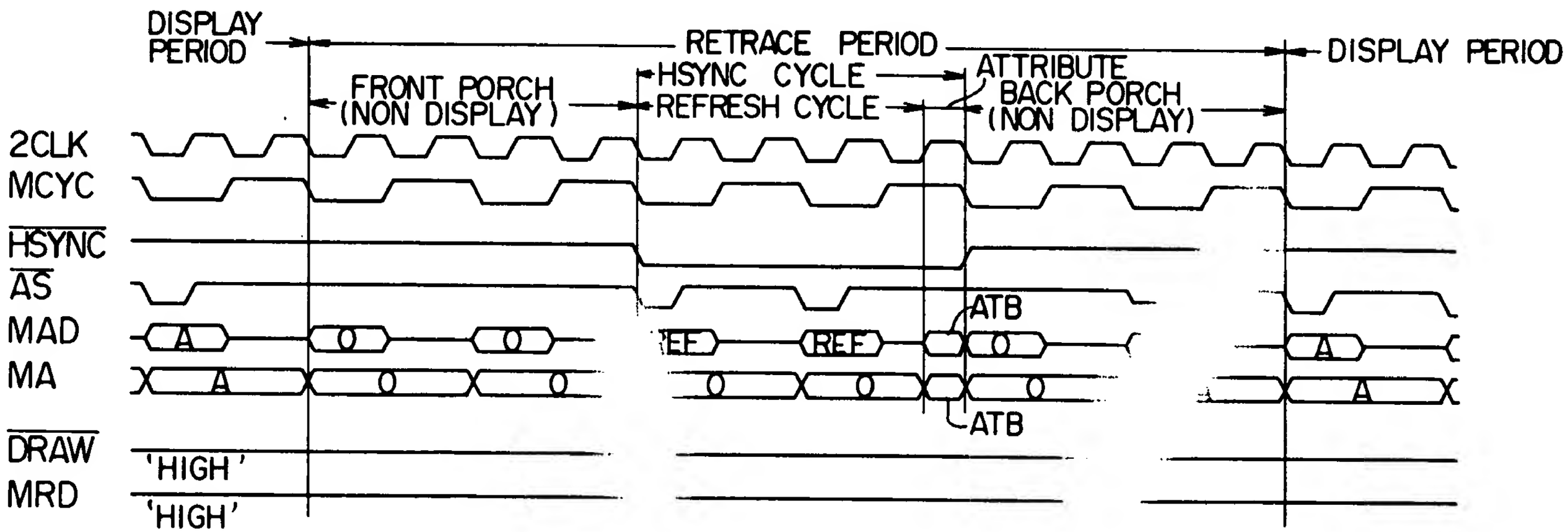

FIG. 11

CUR 1	CUR 0	CURSOR DISPLAY COLOR
0	0	BLACK (VIDEO A - VIDEO D = 0)
0	1	WHITE (VIDEO A - VIDEO D = 1)
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D (VIDEO D IS KEPT UNCHANGED)

FIG. 20b

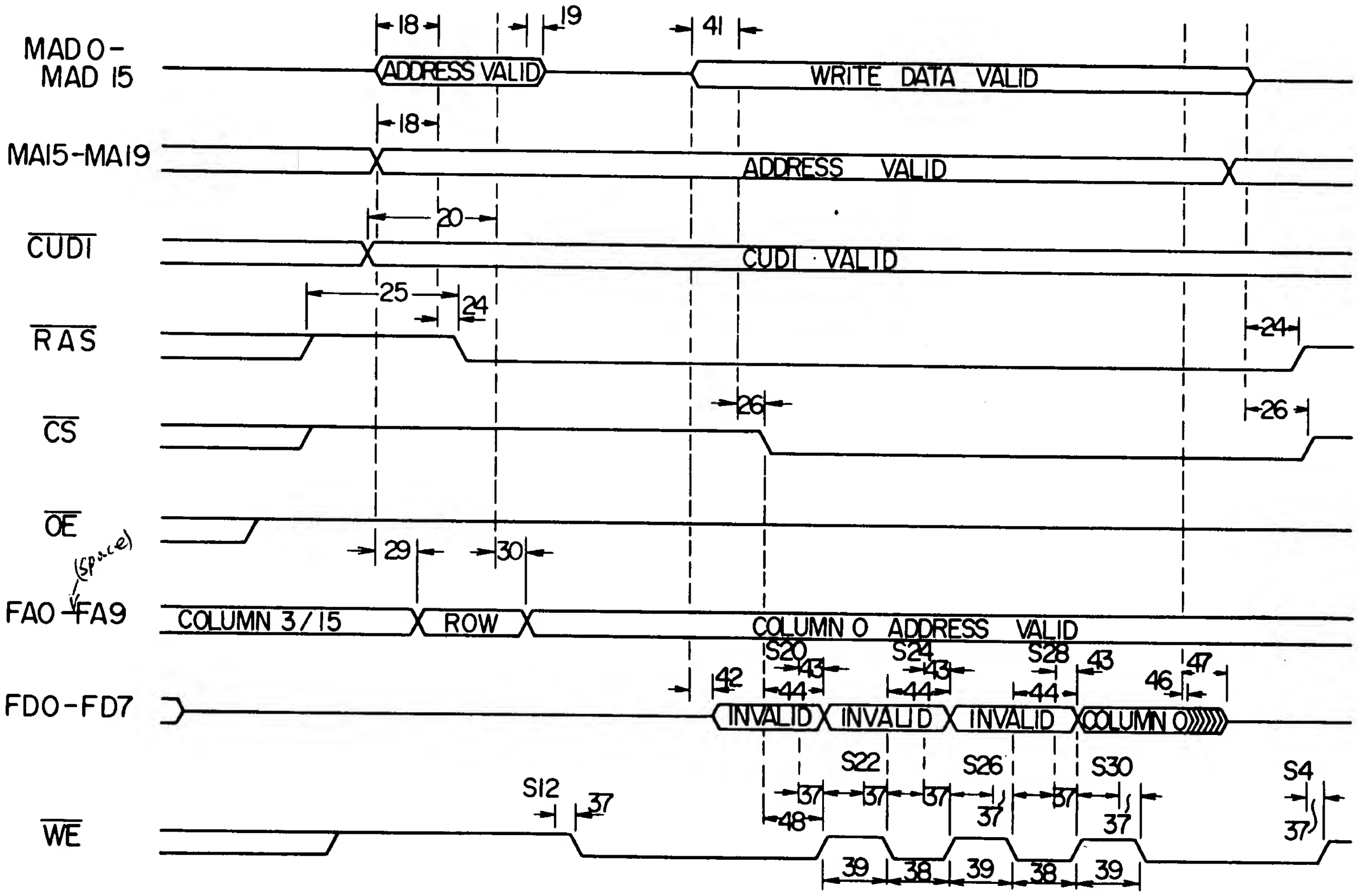
MAD 0-
MAD 15
18
19
41
ADDRESS VALID
WRITE DATA VALID
MA15-MA19
18
ADDRESS VALID
CUDI
20
CUDI VALID
RAS
25
24
24
CS
26
26
OE
29
30
(Space)
FA0-FA9
COLUMN 3/15
ROW
COLUMN 0 ADDRESS VALID
FD0-FD7
S20
S24
S28
42
43
44
43
44
44
43
46
47
INVALID
INVALID
INVALID
COLUMN 0
WE
S12
37
S22
S26
S30
S4
37
37
37
37
37
37
37
48
39
38
39
38
39

FIG. 25

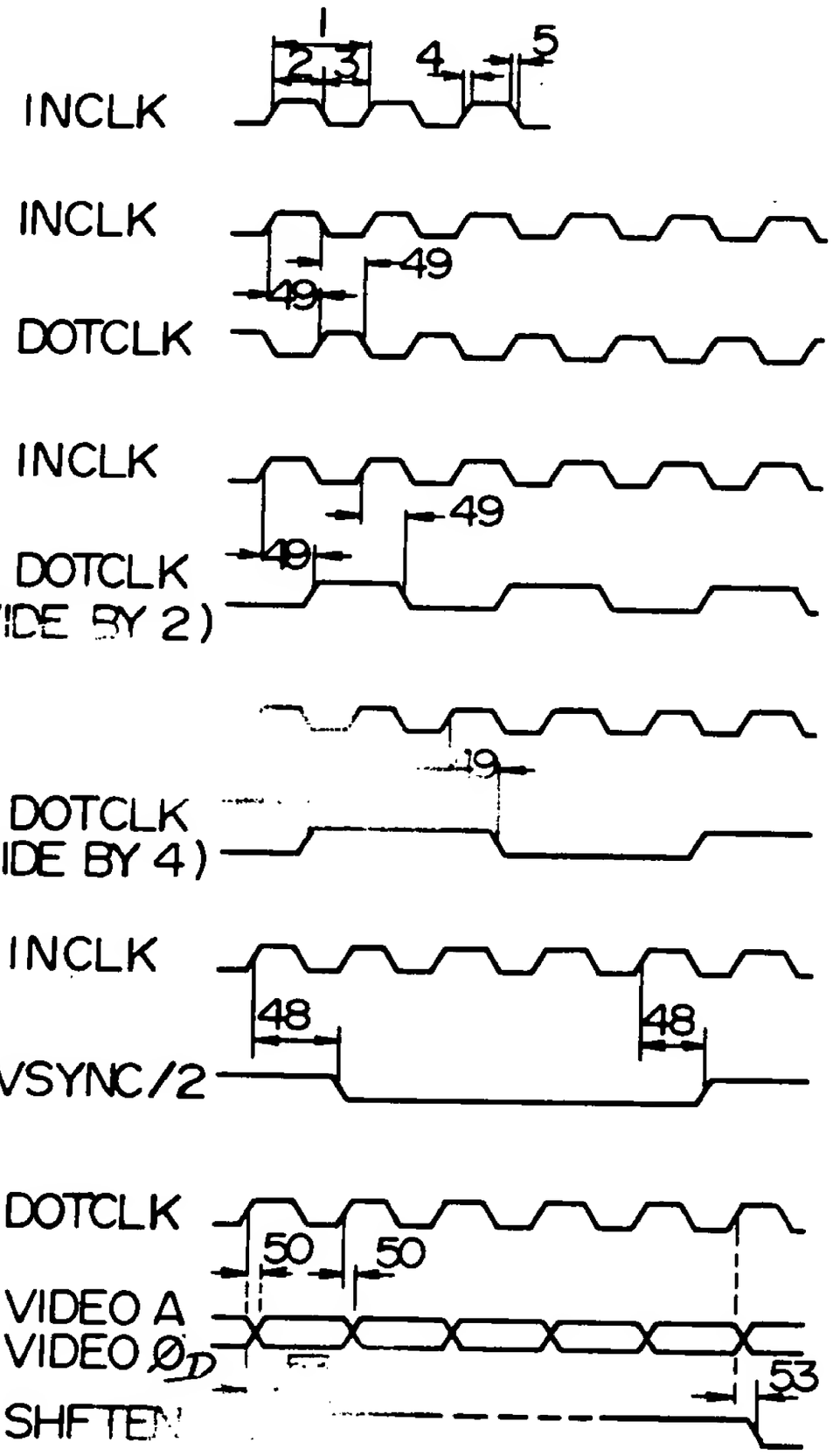
INCLK
1
2
3
4
5
INCLK
49
49
DOTCLK
INCLK
49
49
DOTCLK
(DEVIDE BY 2)
19
DOTCLK
(DEVIDE BY 4)
INCLK
48
48
VSYNC/2
DOTCLK
50
50
VIDEO A
VIDEO ØD
53
SHFTEN

FIG. 26

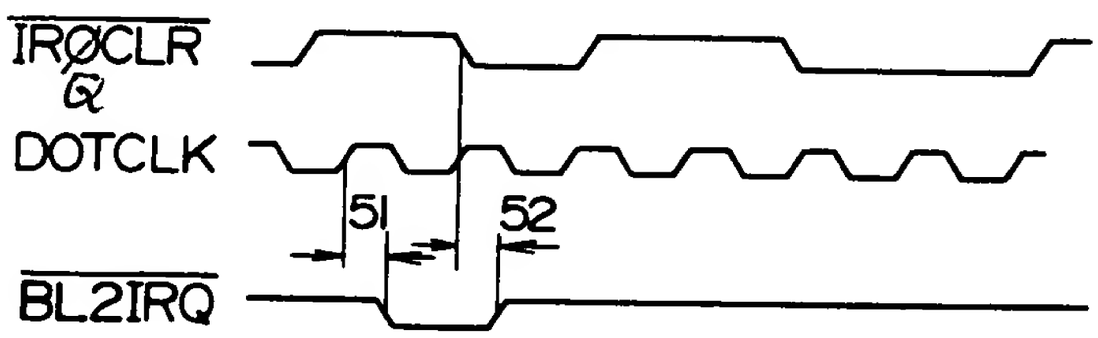
IRØCLR
Q
DOTCLK
51
52
BL2IRQ

FIG. 27

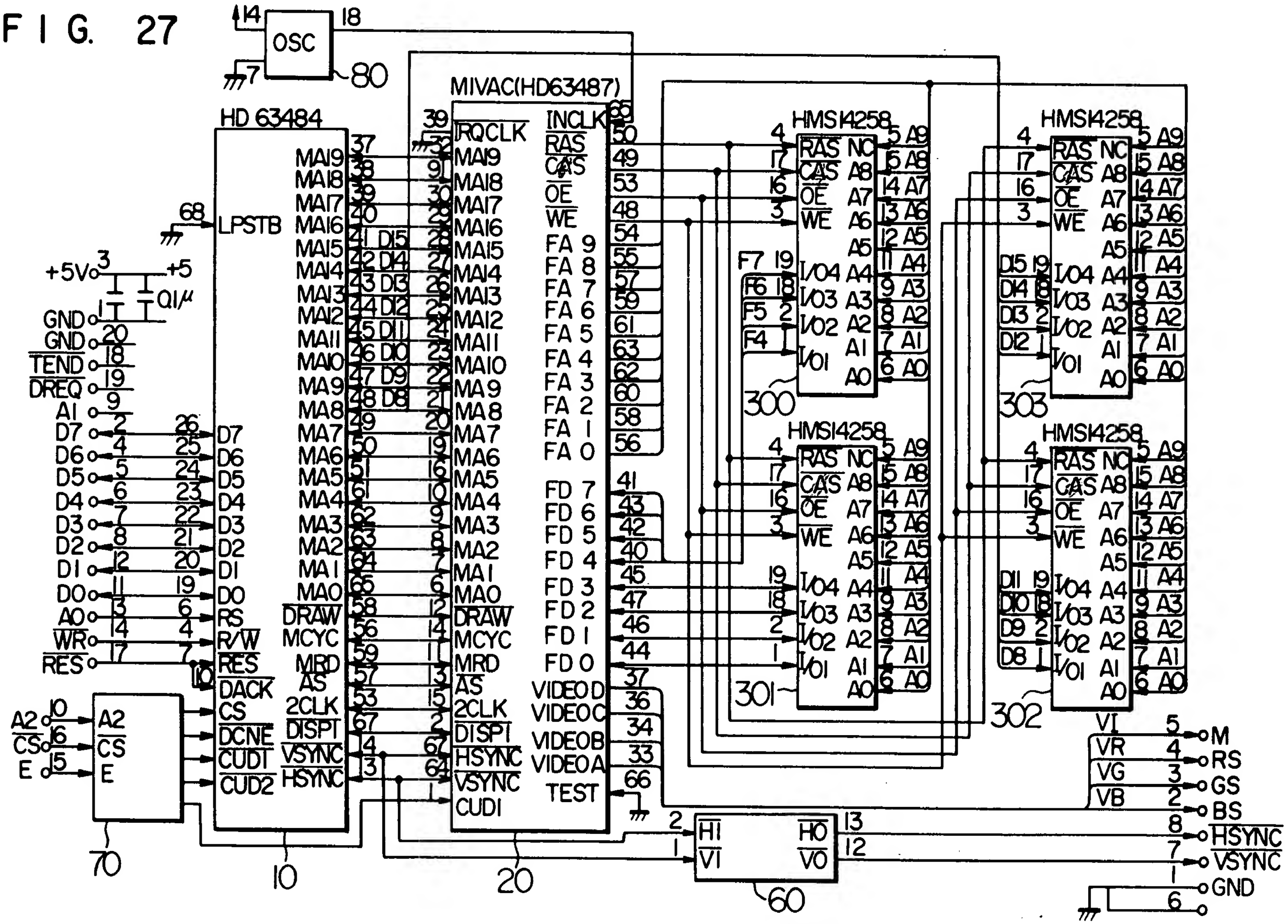
OSC
14
18
7
80
MIVAC(HD63487)
HD 63484
HMS14258
LPSTB
68
+5V
3
+5
0.1μ
GND
1
GND
20
TEND
18
DREQ
19
A1
9
D7
2
D6
4
D5
5
D4
6
D3
7
D2
8
D1
12
D0
11
A0
13
WR
14
RES
17
A2
10
CS
16
E
15
70
10
20
60
INCLK
IRQCLK
RAS
CAS
OE
WE
MA19
MA18
MA17
MA16
MA15
MA14
MA13
MA12
MA11
MA10
MA9
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
DRAW
MCYC
MRD
AS
2CLK
DISPT
VSYNC
HSYNC
CUDI
FA 9
FA 8
FA 7
FA 6
FA 5
FA 4
FA 3
FA 2
FA 1
FA 0
FD 7
FD 6
FD 5
FD 4
FD 3
FD 2
FD 1
FD 0
VIDEOD
VIDEOC
VIDEOB
VIDEOA
TEST
DACK
CS
DCNE
CUDT
CUD2
R/W
RS
D15
D14
D13
D12
D11
D10
D9
D8
F7
F6
F5
F4
I/O4
I/O3
I/O2
I/O1
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
NC
300
301
302
303
HI
VI
HO
VO
VR
VG
VB
M
RS
GS
BS
GND

FIG. 28

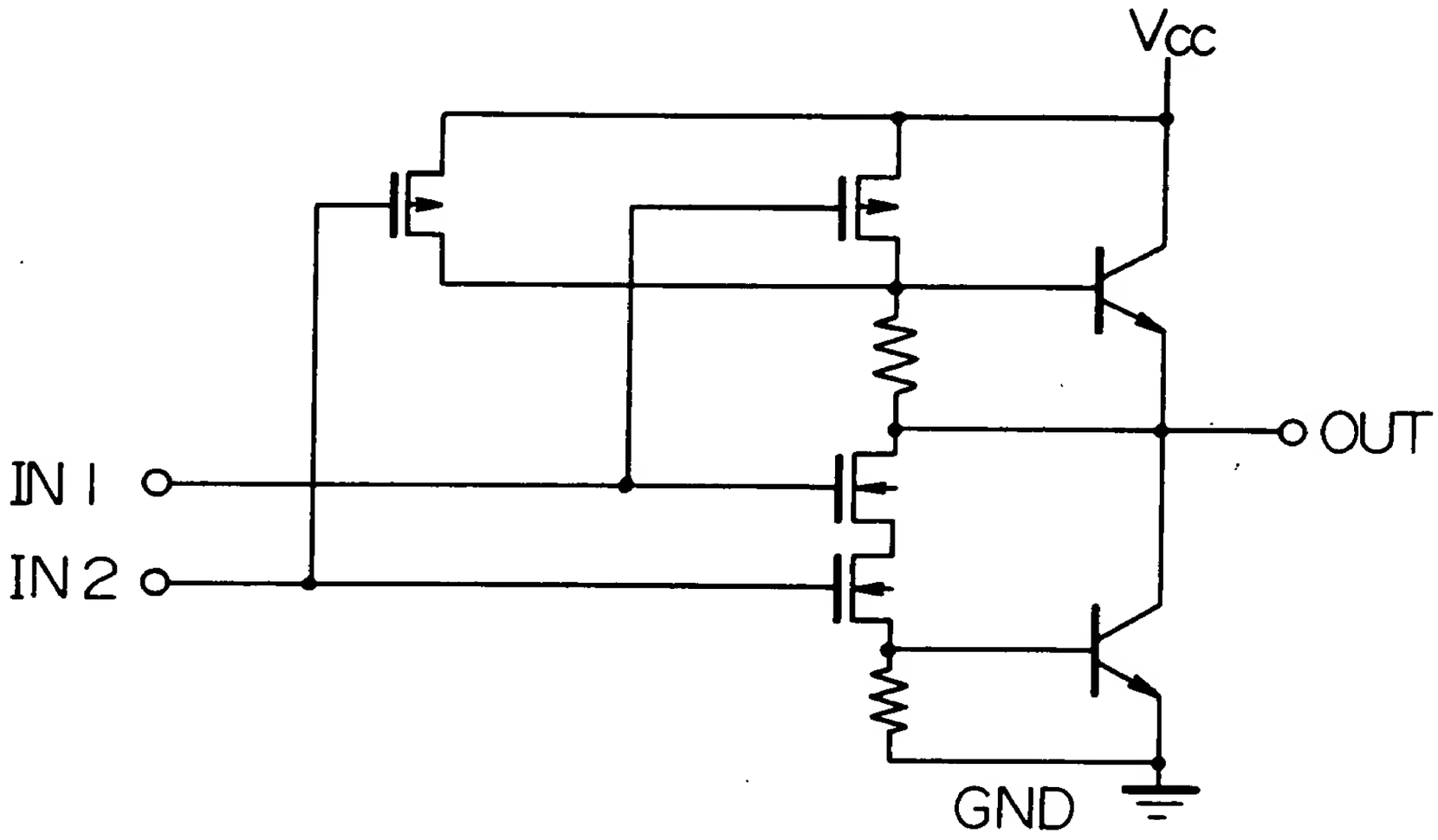

FIG. 29a

FA	4 ACCESSES / MCYC (DRAW, DISPLAY)				16 ACCESSES / 2 MCYCS (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	—	—	MAD 8	NC0	—	—	MAD 8	NC0
8	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1
7	MAD 8	NC2	MA 17	MAD 7	MAD 8	NC2	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC0

[ ] : COLUMN ADDRESS COUNTER